22.1 Overview

Change the second paragraph of 22.1 as follows:

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayers and PHYs for data transfer at 10 Mb/s and 100 Mb/s, and between Station Management (STA) and PHY entities supporting data transfer at 10 Mb/s or above ~~(see 22.2.4)~~. The Clause 45 Management Data Input/Output (MDIO) Interface is recommended in place of the MII Management Interface (see 22.2.4) as the interface between Station Management and PHY entities.

This interface has the following characteristics:

a) It is capable of supporting 10 Mb/s and 100 Mb/s rates for data transfer, and management functions for PHYs supporting data transfer at 10 Mb/s or above (see 22.2.4 or Clause 45).
b) Data and delimiters are synchronous to clock references.
c) It provides independent four bit wide transmit and receive data paths.
d) It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e) It provides a simple management interface.
f) It is capable of driving a limited length of shielded cable.
g) It provides full duplex operation.

22.1.2 Application

Change the first paragraph and lettered list of 22.1.2 as follows:

This clause applies to the interface between MAC sublayer and PHYs, and for some PHY types, between PHYs and Station Management entities. The implementation of the interface may assume any of the following ~~three~~ forms:

. a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.

. b) A motherboard to daughterboard interface between two or more printed circuit boards.

. c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

. d) A logical interface between logic modules within an integrated circuit.

Use of the management interface and registers specified in Clause 45 is recommended for new PHY types and new implementations rather than the management interface and registers specified in 22.2.4. When the MII is not exposed the electrical specifications in this clause are not applicable.

22.1.5 Relationship of MII and GMII

Change the first paragraph of 22.1.5 as follows:

The Gigabit Media Independent Interface (GMII) is similar to the MII. The GMII uses the MII

management interface and register set specified in 22.2.4. Some 100 Mb/s and 1000 Mb/s PHY types use the Clause 45 MDIO Interface. Implementations where the PHY type specifies use of Clause 22 can do so via mappings of Clause 22 registers into the Clause 45 register space. These common elements of operation allow Station Management to determine PHY capabilities ~~for any supported speed of operation~~ and configure the station based on those capabilities. In a station supporting both MII and GMII operation, configuration of the station would include enabling either the MII or GMII operation as appropriate for the data rate of the selected PHY.

22.2.1 Mapping of MII signals to PLS service Primitives and Station Mangement

22.2.4 Management functions

Change the second and third paragraphs of 22.2.4 as follows:

The MII M~~m~~anagement I~~i~~nterface consists of a pair of signals that physically transport the management information across the MII or GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register set can also be read and written through the mapping of the register set to the MDIO Interface (see Clause 45). The register definition specifies a basic register set with an extension mechanism. The MII uses two basic registers. The GMII also uses the same two basic registers and adds a third basic register. Some PHYs define Clause 45 registers other than the mapped MII Management Interface registers.

All PHYs that provide an MII or GMII shall provide either an MII Management Interface or an MDIO Interface.

The MII basic register set consists of two registers referred to as the Control register (Register 0) and the Status register (Register 1). All PHYs that provide an MII Management Interface or the MDIO Clause 22 extension Manageable Device (see 45.2.8) shall incorporate the basic register set. All PHYs that provide a GMII shall incorporate an extended basic register set consisting of the Control register (Register 0), Status register (Register 1), and Extended Status register (Register 15). The status and control functions defined here are considered basic and fundamental to 100 Mb/s and 1000 Mb/s PHYs. Registers 2 through 14 are part of the extended register set. All PHYs that provide a Clause 45 MDIO Interface shall incorporate PHY type specific registers in Clause 45. The format of Registers 4 through 10 are defined for the specific Auto-Negotiation protocol used (Clause 28 or Clause 37). The format of these registers is selected by the bit settings of Registers 1 and 15.

22.2.4.2.16 Extended status

Change ~~the third paragraph of~~ 22.2.4.~~2.16~~ as follows:

When read as a logic one, bit 1.8 indicates that the base register status information is

extended into Register 15. All PHYs supporting 1000 Mb/s operation and the extended register set shall have this bit set to a logic one. When read as a logic zero, bit 1.8 indicates that the extended status is not implemented ~~and that the PHY lacks the ability to perform transmission and reception at 1000 Mb/s~~.

34.1 Overview

Change the second paragraph of 34.1 as follows and ~~change~~ move it down to be the third paragraph:

The Gigabit ~~Ethernet uses the extended~~ Ethernet MAC layer interface~~,~~ connect~~s~~ed through a Gigabit Media Independent Interface layer to Physical Layer entities (PHY sublayers) ~~such as 1000BASE-LX, 1000BASE- SX, and 1000BASE-CX, and 1000BASE-T~~. The set of PHY sublayer specifications include operation over multiple media (various copper cables, fiber optic cables and backplanes). Some of these PHY specifications have been added since development of the initial specifications for operation at 1000 Mb/s, consequently, not all Gigabit Ethernet PHYs are specified in clauses contiguous to this ~~C~~clause.

34.1.2 Physical Layer signaling systems

Change second paragraph of 34.1.2 as follows:

~~The following portion~~ Various clauses of this standard ~~specifies~~comprise a family of Physical Layer implementations for operation at 1000 Mb/s. Each PHY type includes specifications for encoding and decoding of information, and how those encoded data are transmitted on the supported transmission medium or media. These PHY types may share some PHY sublayer components and signaling methods, or may use ~~–~~signaling methods specific to the supported media and applications. ~~1000BASE-T (Clause 40) uses four pairs of balanced copper cabling. 1000BASE-SX (Clause 36, Clause 37, and Clause 38) uses two multimode fibers. There are a number of other PHY types and their associated media.~~

34.1.3 Repeater

Change ~~second paragraph of~~ 34.1.~~3~~2 as follows:

A repeater set (Clause 41) is an integral part of any half duplex Gigabit Ethernet network with more than two DTEs in a collision domain. A repeater set extends the physical system topology by coupling two or more segments. Only one repeater is permitted within a single collision domain. Some Gigabit Ethernet PHY types only support full duplex operation. Topologies composed of full duplex only devices do not allow repeaters.~~).~~

35.1.2. Application

Change the first paragraph of 35.1.2 as follows:

This clause applies to the interface between the MAC and PHYs, and between PHYs and Station Management entities. The implementation of the interface is primarily intended as a chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit

board. A motherboard-to-daughterboard interface between two or more printed circuit boards is not precluded. The use of parts of the GMII (e.g., data paths, but not the Clause 22 management interface or associated Clause 22 management registers), and the use of the GMII as an interface between logic modules on the same chip is not precluded.

35.1.3. Rate of Operation

Change the second paragraph of 35.1.3 as follows:

PHYs that provide a GMII shall support 1000 Mb/s operation, and may support additional rates using other interfaces (e.g., MII). PHYs must report the rates at which they are capable of operating via a ~~the~~ management interface, (e.g., as described in Clause 22 ~~and~~ or Clause 45)~~22.2.4~~. Reconciliation sublayers that provide a GMII shall support 1000 Mb/s and may support additional rates using other interfaces.

35.2.5 Management functions

Change 35.2.5 as follows:

The GMII shall use either the MII management register set specified in 22.2.4 or 45.2. Which register set is used and the~~The~~ detailed description of some management registers are dependent on the PHY type and, if applicable, the type of auto-negotiation used~~are specified in either 28.2.4 or 37.2.5~~.